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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,921	02/25/2004	Mats Lindstrom	109822-100	4977
7590 06/28/2006			EXAMINER	
Troy M. Schmelzer HOGAN & HARTSON L.L.P. 500 South Grand Avenue, Suite 1900 Los Angeles, CA 90071			TRAN, KHAI	
			ART UNIT	PAPER NUMBER
			2611	

DATE MAILED: 06/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

8

Office Action Summary	Application No. 10/786,921	Applicant(s) LINDSTROM ET AL.	
	Examiner KHAI TRAN	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 22-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 22-26, 31 is/are rejected.
- 7) ☒ Claim(s) 27-30 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The preliminary amendment filed 2/25/2004 has been entered. Claims 1-21 have been cancelled. Claims 22-32 are pending in this Office action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 22-26, 31, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Taketoshi et al (U.S. Pat. 5,389,898) hereinafter Taketoshi.

Regarding claim 22, Taketoshi discloses a method for calibrating a local oscillator as shown in Figures 1 and 7, comprising a plurality of voltage controlled oscillators (VCO 1, VCO 2, VCO 3), integrated on a single semiconductor chip for use in a broadband tuner, comprising the steps of: selecting an initial frequency (a target frequency, see col. 4, lines 58-64); checking a lock detect output of a phase-locked loop iteratively for frequencies above and below the initial frequency to determine a lower edge and an upper edge of a set of frequencies to which a current voltage controlled oscillator can be tuned; and performing (see col. 4, lines 40-64 illustrating that the VCO1, VCO2, and VCO3 have different mean frequencies and their oscillator frequency is controlled according to the voltage value of the V.sub.cnt from the filter 2. Of these three VCO's the VCO1 has the highest mean frequency and the VCO3 is given the lowest. The multiplexer 4 is a selector used to select one of the outputs of the VCO1,

Art Unit: 2611

VCO2, and VCO3 under parallel running, as a basic clock signal (ϕ_0). Upon receiving a pulse of the signal UP or the signal DOWN twice in succession from the phase detector 1, the counter 5 delivers a shift signal to the shift register 6. The shift register 6 is a register capable of storing selection control data for the multiplexer 4 to select a desired output. Such data is updated upon application of a shift signal from the counter 5. The frequency divider 7 divides the frequency of the ϕ_0 to generate the ϕ_2 with a 50% duty ratio. This ϕ_2 is fed back to the phase detector 1 as one input thereof. Based on either an external preset signal or a selection control signal, the multiplexer 4 selects one of the outputs of the VCO's. An external preset signal is a preset signal which allows the multiplexer 4 to select one of the VCO1, VCO2, and VCO3 before the PLL becomes activated. This makes it possible for the PLL to start tracking a target frequency at any operating point).

Regarding claim 23, Taketoshi discloses wherein the checking step is performed A binary search algorithm (using pulses of the signal Up and signal DOWN for selecting VCO1, VCO2, or VCO3).

Regarding claim 24, Taketoshi discloses wherein the binary search uses initial step size between ten and fifty percent of the predicted bandwidth of the current voltage controlled oscillator (col. 3, lines 32-52).

Regarding claim 25, Taketoshi discloses wherein the selecting step uses a predicted center frequency for the current voltage controlled oscillator (using a divider 7 wherein a divide ratio of the frequency divider is set to $1/n$).

Regarding claim 26, Taketoshi discloses step of calculating breakpoints between each voltage oscillator from a set of upper and lower edges thereby minimizing the probability of one of the voltage controlled being used to tune to a frequency near either the upper or lower edge of that voltage controlled oscillator's tuning range (see Figures 2-6, and using a counter 5).

Regarding claim 32, Taketoshi discloses wherein the method is performed once at start-up (col. 6, lines 20-45).

Claim 32 is similar to claims 1, 25-26. Therefore, claim 32 is rejected under a similar rationale.

Allowable Subject Matter

4. Claims 27-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: Taketoshi fails to disclose or suggest the limitations of generating a look-up table for identifying which voltage controlled oscillator to use given a specified carrier frequency; and wherein the generating step further comprises generating a set of divide ratios to apply to an output of the local oscillator for inclusion in the look-up table.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Art Unit: 2611

Pierce (U.S. Pat. 4,446,564) discloses a phase-locked-loop frequency synthesizer.

Ueno et al (US 2002/0001361 A1) disclose a semiconductor integrated circuit.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHAI TRAN whose telephone number is (571) 272-3019. The examiner can normally be reached on 7:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JAY PATEL can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



KHAI TRAN
Primary Examiner
Art Unit 2611

KT
June 22, 2006